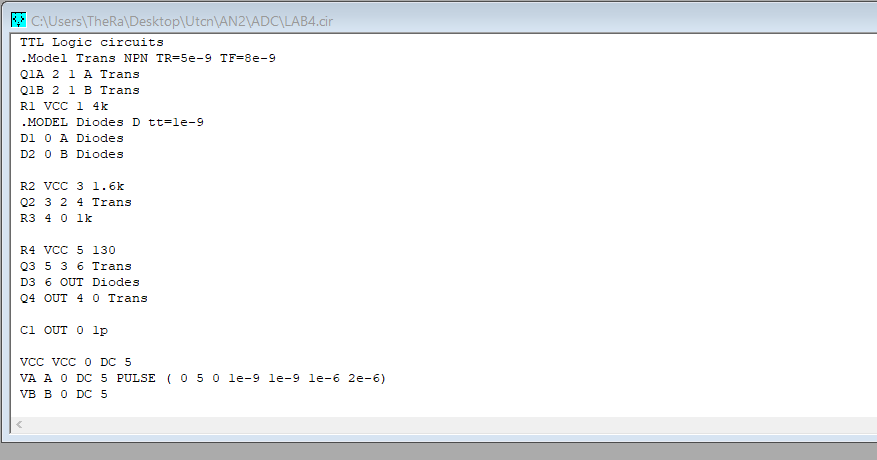
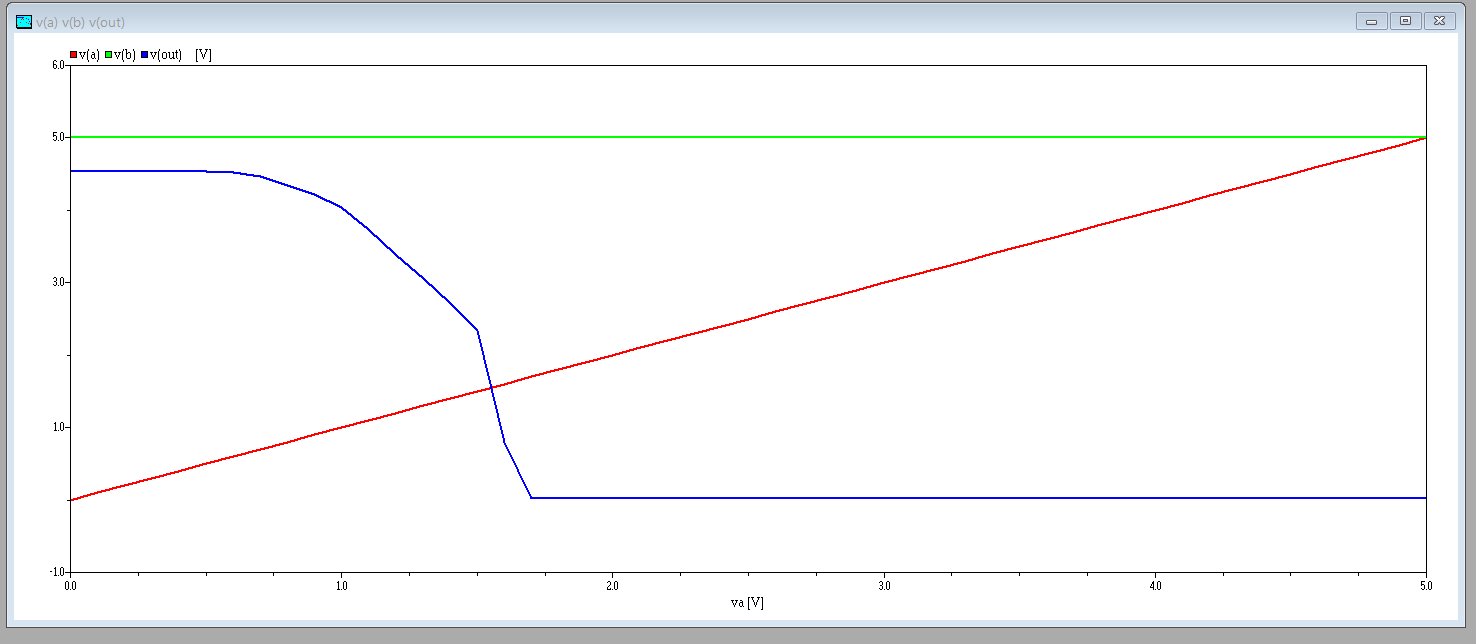
In this lab we implemented a NAND gate using TTL. The circuit is formed with 4 Transistors, 4 Rezistors and 3 Diodes. If one of the inputs is connected to ground, Q1 is Saturated and Q2 is in cut-off stage. Low voltage in Q2 emitter determine blocking of the Q4 Transistor. Q3 transistor will be in conduction and output will be 1.

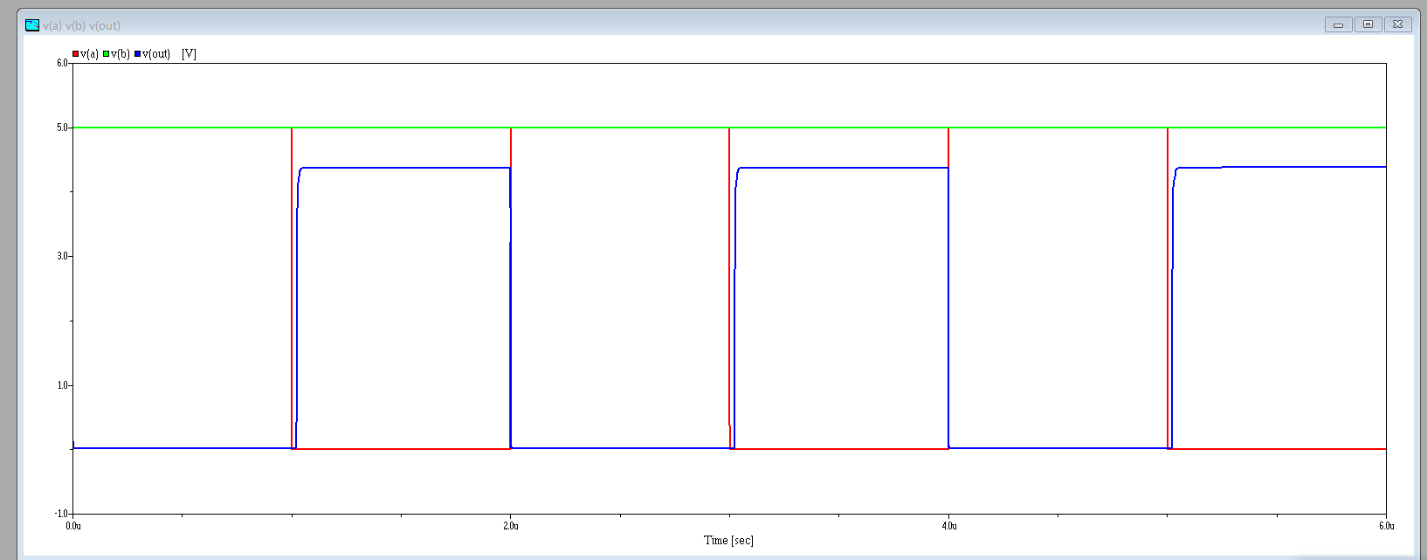
**CODE :**



**DC Analysis :**



**TR Analysis :**



We used a pulse in VA to see the diferences in how the current flucates in order to get the NAND gate/